SIO-4 SERIAL INTERFACE DATA

INSTALLATION

The SIO-4 comes installed as part of the 380Z disk system. If your SIO-4C (cassette based verision of the SIO-4) is not installed in your system then follow the normal procedure for plugging an extra board into the 50 way bus, and mount the external 25 way connector in a suitable cut-out in the rear panel, after removing a blanking plate. The ten way connector plugs into the left hand end of the board, at the rear that is. If the cable in it is multi coloured then the plug must be inserted with the brown wire near the edge of the board. If the cable is grey, then the red stripe must be near the edge of the board.

CONNECTION

The SIO-4 I/O connector is a 25 way 'D Submin.' female socket mounted on the rear panel of the 380Z. **WARNING**: if there is more than one 25 way 'D type' connector on the rear panel it is likely that one of these is a parallel I/O port connector. On later 380Z's the relevant connector is marked "S4". Connecting an RS232 serial device to the parallel I/O port will damage your equipment, so determine which is the connector you want before connecting.

OPERATION

The SIO-4 is selected as the system lineprinter option either on power on, after RESET, or from the front panel. After power on or RESET type the letter O (for Options), L (for lineprinter), 4 (for output device handler 4) and then a number between 0 and 6 for the required Baud rate, as given by the following table:

0 = 110 Baud
1 = 300 Baud
2 = 600 Baud
3 = 1200 Baud
4 = 2400 Baud
5 = 4800 Baud
6 = 9600 Baud

If you require a non-standard baud rate you will have to write and link your own handler to COS - for guidance refer to the 'SIO-4 handler' in the COS listing.

RESET will always cancel any existing lineprinter option selection, so repeat this procedure after reset. If you did not select your options immediately after power on or RESET, you can select them at any time by

going into 'front panel' by typing Control-F, and the O, L, 4, etc., as above. You can then return from front panel mode to the program or mode you were in by typing K. Note however that K will often appear to have little effect as the mode you were in will usually be 'waiting for an input of some kind' and you will simply return to this waiting.

OUTPUTTING

Once the option has been selected, high level software lineprinter commands will be directed to the SIO-4 device. For details of these commands refer to the relevant manual. Outputting to the SIO-4 from machine language, once the option has been selected, can be achieved by using an F705 call, with the ASCII code in register A.

INPUTTING

Once the option has been selected, an SK4IN call can be used as an SIO-4 reader routine and SK4TL can be used to test the status; refer to your COS literature.

CONNECTING TO A DEVICE WITH A READY LINE

Buffered printers and some other devices have an output which must be used to tell the 380Z that the receiving device is not ready to receive data. For these devices connection must be made to wire 5 on the 10 way cable which connects the SIO to the rear panel sockets. When shipped this wire, the fifth from the side nearest the outer edge of the board, is either not connected or is connected to pin 4 of the 25 way connector. It is very likely that the peripheral will not use pin 4 for its busy signal as their are a number of ways of interpreting RS 232 functions, and you will have to make suitable connections with reference to your peripherals data sheet.

ADVANCED USE of the SIO:

The SIO uses an 8251 universal asynchronous receiver/transmitter. A copy of the 8251 datasheet is at the end of this data sheet. There are several inputs and outputs to the 8251 which are buffered and brought out to the 10 way cable which some users might like to know about. Here is the wiring list for the 10 way cable. Wire one (pin one on the 10 way connector) is the wire nearest the outer edge of the interface board. Function names refer to the relevant 8251 pin.

Wire 1: TxD' Transmitted data out (Brown)

Wire 2: signal ground (Red)

Wire 3: RxD' received data in (Orange)

Wire 4: direct digital ground (Yellow)

Wire 5: DSR data set reading input (Green)

Wire 6: +5 Volts (Blue)

Wire 7: DTR data terminal ready output (Violet)

Wire 8: RTS ready to send output (Grey)

Wire 9: minus twelve volts (White)

Wire 10: CTS Clear to send output (Black)

The inputs to the 8251 integrated circuit (IC) are buffered and inverted by a 75189 IC, the outputs from the 8251 are inverted and buffered by an 75188 IC.

HANDLER PROGRAMMING NOTES

The device is access via Z80 port input/output instructions. The base address of the set of ports used varies. On an SIO-4 supplied in conjunction with an FDS system the base address "F SIO" is E8, on an MDS system it is C8. On an SIO-4C supplied in a cassette system it is C8, and on a disk machine, the base address will be whichever of the above two has not been used by the SIO-4. Other base address can be set up by suitable track cutting and wire-wrap linking on the board, to allow addition of interfaces. A typical SIO handler is given at the end of this datasheet. Note that this does not include baud rate set up, and that "F SIO" in this case is C8.

SIO-4 CONNECTIONS

CINCH 25 WAY FEMALE Pin No.	COLOUR
1	NC
2	ORANGE
3	BROWN
4	GREEN
5	NC
6	NC
7	RED
8	NC
1,8-25	NOT CONNECTED

NC - No connection

From 7th July,1980.

The SIO-4 has been wired in three ways during its life. Pins 2, 3 and 7 have never altered, these are Data In, Data Out and Ground respectively.

Early SIO-4 leads had only pins 2, 3 and 7 wired. The next wiring method included GREEN to pin 4 in addition to the data and ground, this was to provide a Busy line, and matches that wired on the QUME Sprint 5 daisywheel printer. Type 3, the current one, matches type 2 we have reverted to this after briefly wiring according to V24 in which pins 2, 3, 4, 5, 6, 7, 8 were wired, this caused problems with Teletypes and since the connections do not appear to match many printers we have opted for the simple case with the addition of a busy line.

SIO-4 INTERFACE RML Z80 ASS V 3.0 A

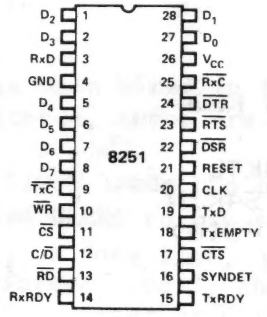
```
                    2357 *H SIO-4 INTERFACE
                    2358
                    2359 ;SI4 - OUTPUT TO SERIAL INTERFACE ON DISK
                    2360 ;CONTROLLER
                    2361
EBD9 F724           2362 SI4:    EMT     SAVEA
EBDB 4F             2363         LD      C,A
EBDC DBC9           2364 SI4A:   IN      A,(FSIO+1)      ;WAIT UNTIL NOT BUSY
EBDE CB7F           2365         BIT     7,A
EBE0 2005           2366         JR      NZ,SI4B
EBE2 CD02EC         2367         CALL    LSTBRK
EBE5 18F5           2368         JR      SI4A
EBE7 CB47           2369 SI4B:   BIT     0,A             ;WAIT UNTIL TX RDY
EBE9 28F1           2370         JR      Z,SI4A
EBEB 79             2371         LD      A,C
EBEC D3C8           2372         OUT     (FSIO),A        ;SEND BYTE
EBEE C9             2373         RET
                    2374
                    2375 ;S4KTL - TEST SIO-4 KBD FOR CHAR WAITING
                    2376 ;RETURN ZERO IF NO CHAR, ELSE 0FFH
                    2377
EBEF DBC9           2378 .S4KTL: IN      A,(FSIO+1)      ;RD STATUS
EBF1 CB4F           2379         BIT     1,A
EBF3 3E00           2380         LD      A,0
EBF5 C8             2381         RET     Z
EBF6 3D             2382         DEC     A
EBF7 C9             2383         RET
                    2384
                    2385 ;S4KIN - READ SIO-4 KBD
                    2386
EBF8 CDEFEB         2387 .S4KIN: CALL    .S4KTL          ;WAIT FOR CHAR
EBFB 28FB           2388         JR      Z,.S4KIN
EBFD DBC8           2389         IN      A,(FSIO)
EBFF E67F           2390         AND     7FH             ;STRIP PARITY
EC01 C9             2391         RET
                    2392
                    2393 ;LSTBRK - ALLOW EXIT FROM PRINTER OFF-LINE
                    2394 ;BY CTRL C
                    2395
EC02 F71E           2396 LSTBRK: EMT     KBDTC           ;TEST KBD .
EC04 FE03           2397         CP      CTRLC
EC06 CAF8E3         2398         JP      Z,GETC          ;ECHO ^C, REBOOT
EC09 C9             2399         RET
```

8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1, 16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
- **Baud Rate —DC to 56k Baud (Sync Mode)**
  DC to 9.6k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs Are TTL Compatible**
- **Single 5 Volt Supply**
- **Single TTL Clock**

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

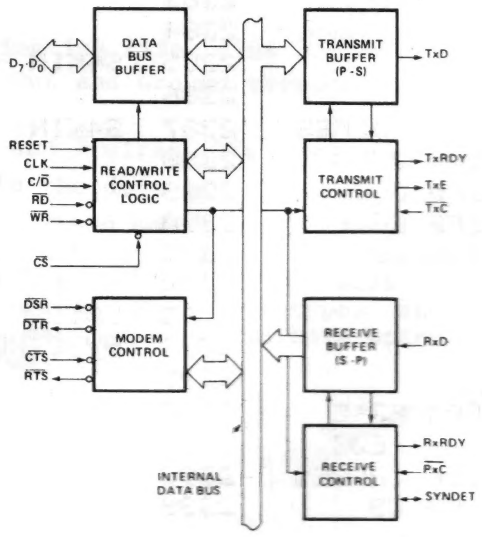
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



8251 BASIC FUNCTIONAL DESCRIPTION

General

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 8080 Microcomputer System. Like other I/O devices in the 8080 Microcomputer System its functional configuration is programmed by the systems software for maximum flexibility. The 8251 can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8251 to the 8080 system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the 8080 CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer.

Read/Write Control Logic

This functional block accepts inputs from the 8080 Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for device functional definition.

RESET (Reset)

A "high" on this input forces the 8251 into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251 to program its functional definition. Minimum RESET pulse width is 6 t_{CY}.

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter clock inputs for synchronous mode (4.5 times for asynchronous mode).

$\overline{WR}$ (Write)

A "low" on this input informs the 8251 that the CPU is outputting data or control words, in essence, the CPU is writing out to the 8251.

$\overline{RD}$ (Read)

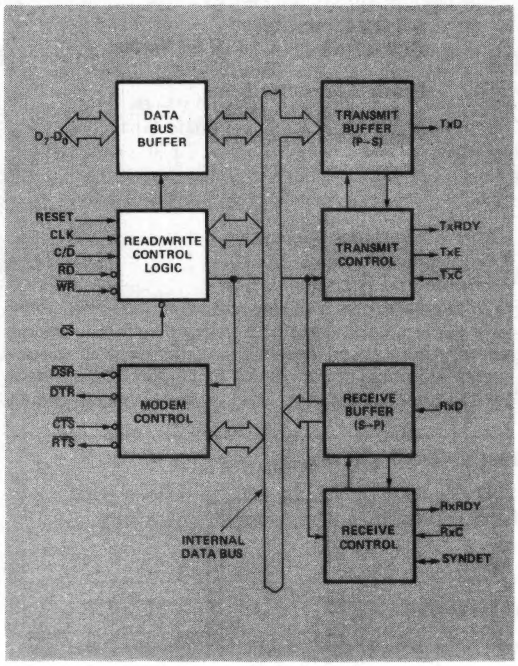
A "low" on this input informs the 8251 that the CPU is inputting data or status information, in essence, the CPU is reading from the 8251.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs informs the 8251 that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL 0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8251. No reading or writing will occur unless the device is selected.



C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251 ⇒ DATA BUS
0	1	0	0	DATA BUS ⇒ 8251
1	0	1	0	STATUS ⇒ DATA BUS
1	1	0	0	DATA BUS ⇒ CONTROL
X	1	1	0	DATA BUS ⇒ 3-STATE
X	X	X	1	DATA BUS ⇒ 3-STATE

Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is general purpose in nature. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251 to transmit data (serial) if the Tx EN bit in the Command byte is set to a "one."

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

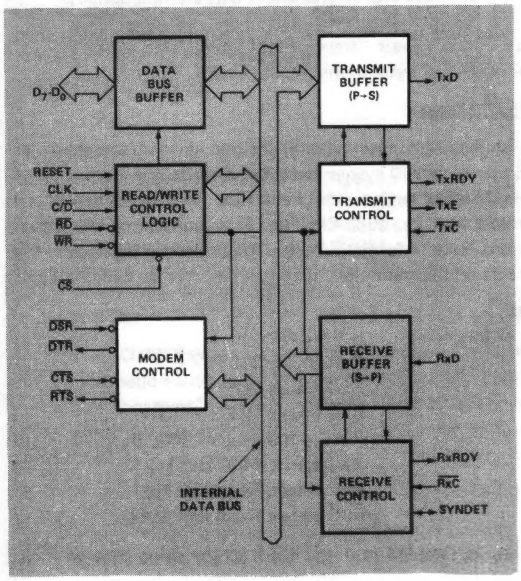
TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or for the Polled operation the CPU can check TxRDY using a status read operation. TxRDY is automatically reset when a character is loaded from the CPU.

TxE (Transmitter Empty)

When the 8251 has no characters to transmit, the TxE output will go "high". It resets automatically upon receiving a character from the CPU. TxE can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode. TxE is independent of the TxEN bit in the Command instruction.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as "fillers". TxE goes low as soon as the SYNC is being shifted out.



$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{TxC}$ is equal to the actual Baud Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{TxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x or 64x the Baud Rate.

For Example:

If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz (1x)
$\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{TxC}$ equals 7.04 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to the RxD pin.

Receiver Control

This functional block manages all receiver-related activities.

RxRDY (Receiver Ready)

This output indicates that the 8251 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or for Polled operation the CPU can check the condition of RxRDY using a status read operation. RxRDY is automatically reset when the character is read by the CPU.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{RxC}$ is equal to the actual Baud Rate (1x). In Asynchronous Mode, the frequency of $\overline{RxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x or 64x the Baud Rate.

For Example:
If Baud Rate equals 300 Baud,
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).
If Baud Rate equals 2400 Baud,
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

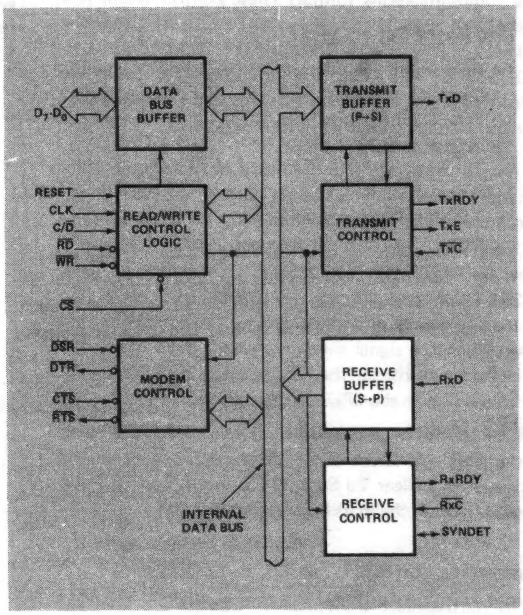
Data is sampled into the 8251 on the rising edge of $\overline{RxC}$.

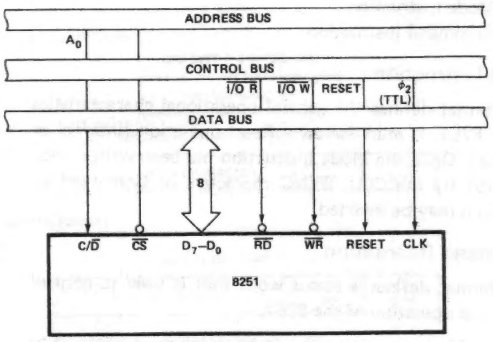
NOTE: In most communications systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)

This pin is used in SYNChronous Mode only. It is used as either input or output, programmable through the Control Word. It is reset to "low" upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251 has located the SYNC character in the Receive mode. If the 8251 is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input, (external SYNC detect mode), a positive going signal will cause the 8251 to start assembling data characters on the falling edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. The duration of the high signal should be at least equal to the period of $\overline{RxC}$.





8251 Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize the 8251 to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD PARITY etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251 is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251 is ready to receive a character. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251. On the other hand, the 8251 receives serial data from the MODEM or I/O device, upon receiving an entire character the RxRDY output is raised "high" to signal the CPU that the 8251 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU read operation.

The 8251 cannot begin transmission until the TxEN (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send (CTS) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251

Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

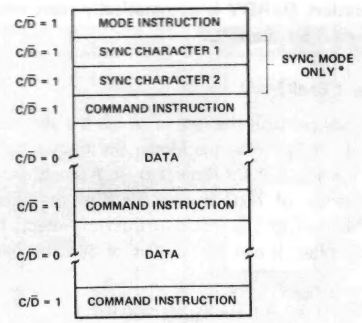
This format defines the general operational characteristics of the 8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the CPU, SYNC characters or Command instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251.

Both the Mode and Command instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.

All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format a bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.



*The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

Typical Data Block

Mode Instruction Definition

The 8251 can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251 the designer can best view the device as two separate components sharing the same package. One Asynchronous the other Synchronous. The format definition can be changed "on the fly" but for explanation purposes the two formats will be isolated.

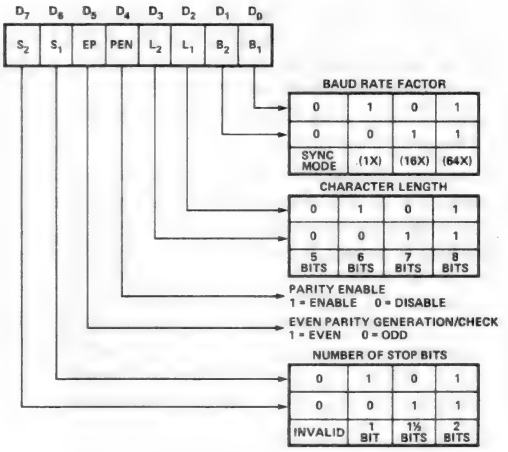
Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

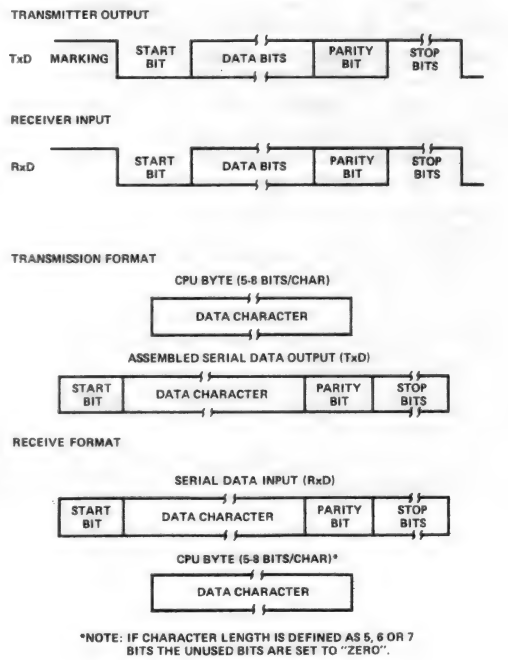
When no data characters have loaded into the 8251 the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. This character is then loaded into the parallel I/O buffer of the 8251. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurrence of any of these errors will not stop the operation of the 8251.



Mode Instruction Format, Asynchronous Mode

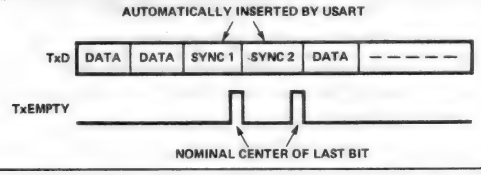


Asynchronous Mode

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251 which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251 with a character before the 8251 becomes empty, the SYNC characters (or character if in single SYNC word mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251 is empty and SYNC characters are being sent out. TxEMPTY goes low when SYNC is being shifted out (See Figure below). The TxEMPTY pin is internally reset by the next character being written into the 8251.



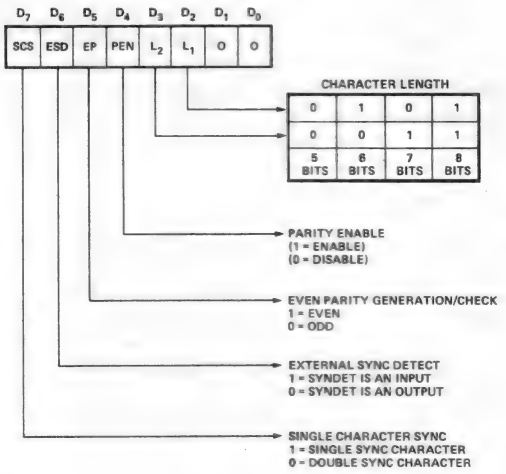
Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the internal SYNC mode has been programmed, the receiver starts in a HUNT mode. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is continuously compared with the first SYNC character until a match occurs. If the 8251 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ.

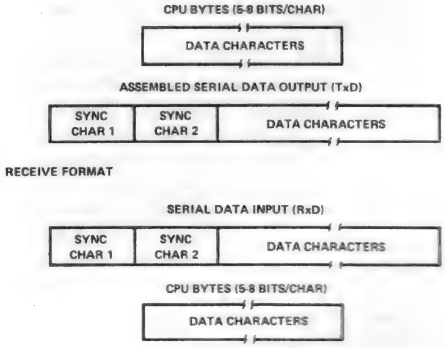
In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin. The high level can be removed after one $\overline{RxC}$ cycle.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost.



Mode Instruction Format, Synchronous Mode

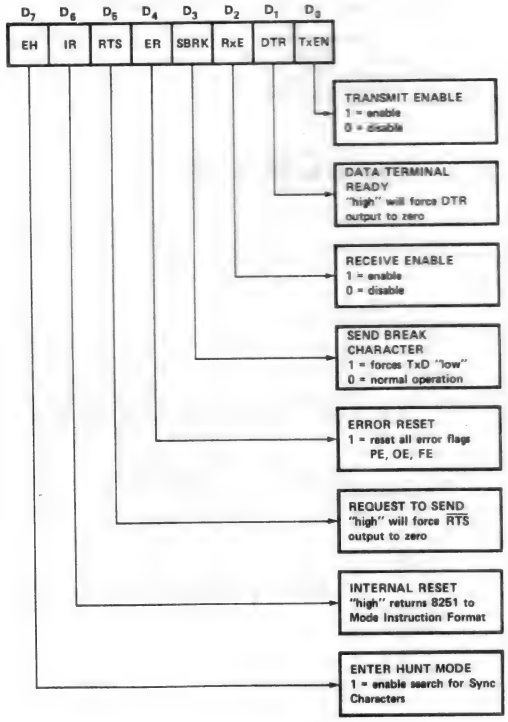


Synchronous Mode, Transmission Format

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251 has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251 and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D}$ = 1) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.



Command Instruction Format

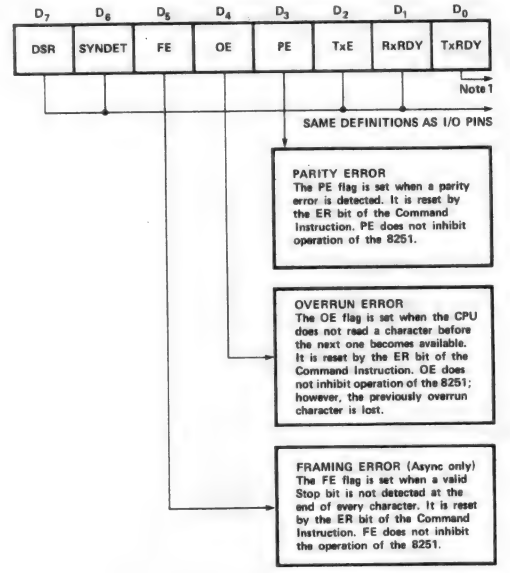
STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251 has facilities that allow the programmer to "read" the status of the device at any time during the functional operation.

A normal "read" command is issued by the CPU with the C/D input at one to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251 can be used in a completely Polled environment or in an interrupt driven environment.

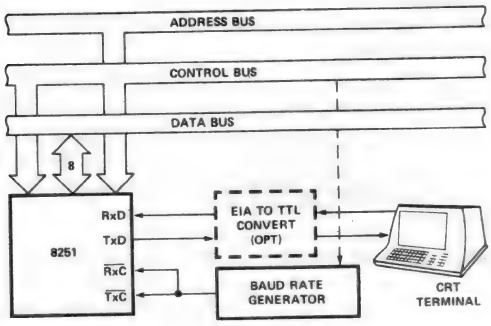
Status update can have a maximum delay of 16 clock periods.



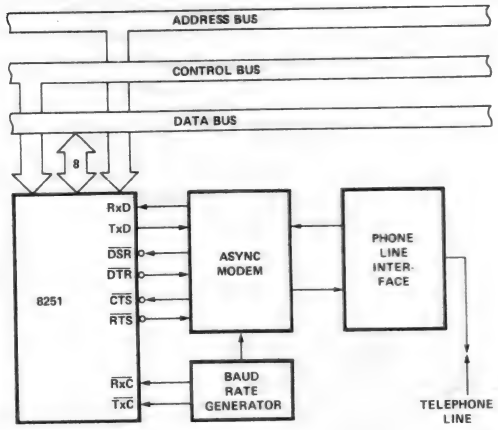
Status Read Format

Note 1: TxRDY status bit has similar meaning as the TxRDY output pin. The former is not conditioned by CTS and TxEN; the latter is conditioned by both CTS and TxEN.
i.e. TxRDY status bit = DB Buffer Empty
TxRDY pin out = DB Buffer Empty • CTS • TxEN

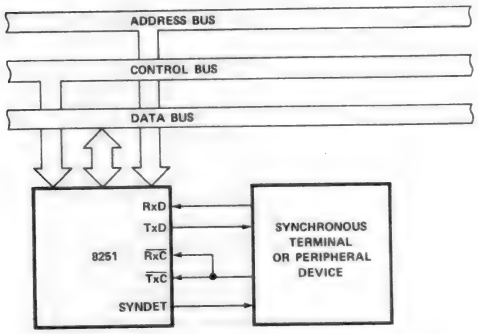
APPLICATIONS OF THE 8251



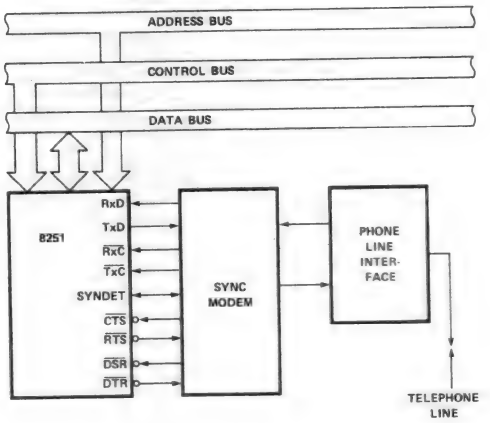
Asynchronous Serial Interface to CRT Terminal, DC-9600 Baud



Asynchronous Interface to Telephone Lines



Synchronous Interface to Terminal or Peripheral Device



Synchronous Interface to Telephone Lines

Absolute Maximum Ratings*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Characteristics:

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100μA
I_{DL}	Data Bus Leakage			–50 10	μA μA	V_{OUT} = .45V V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	μA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	

Capacitance:

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

TEST LOAD CIRCUIT:

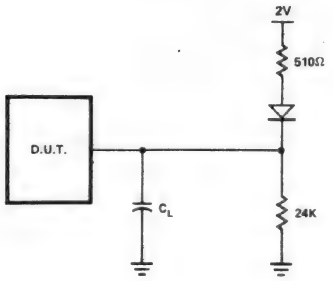
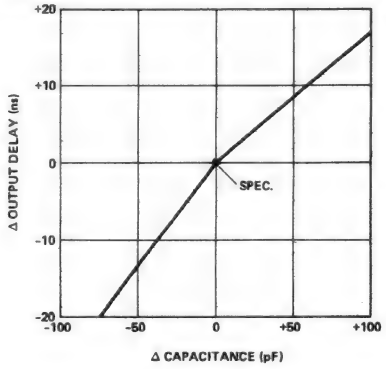


Figure 1.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (dB)



A.C. Characteristics:

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

BUS PARAMETERS: (Note 1)

READ CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/D)	50		ns	
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/D)	5		ns	
t_{RR}	$\overline{READ}$ Pulse Width	430		ns	
t_{RD}	Data Delay from $\overline{READ}$		350	ns	C_L = 100 pF
t_{DF}	$\overline{READ}$ to Data Floating		200	ns	C_L = 100 pF
		25		ns	C_L = 15 pF
t_{RV}	Recovery Time Between WRITES (Note 2)	6		t_{CY}	

WRITE CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	Address Stable Before $\overline{WRITE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	200		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		ns	

NOTES: 1. AC timings measured at V_{OH} = 2.0, V_{OL} = .8, and with load circuit of Figure 1.
2. This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

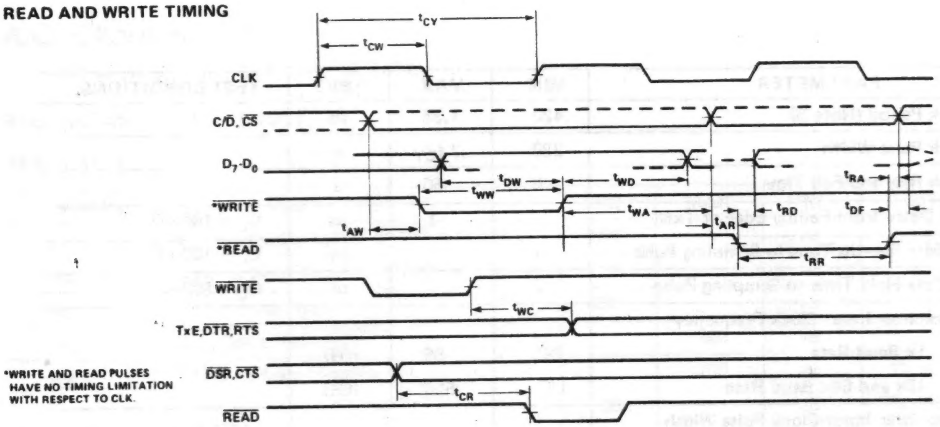
OTHER TIMINGS:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{CY}	Clock Period (Note 3)	.420	1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220	.7 t_{CY}	ns	
t_R, t_F	Clock Rise and Fall Time	0	50	ns	
t_{DTx}	TxD Delay from Falling Edge of TxC		1	μs	C_L = 100 pF
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	C_L = 100 pF
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	C_L = 100 pF
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	56	KHz	
	16x and 64x Baud Rate	DC	520	KHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	56	KHz	
	16x and 64x Baud Rate	DC	520	KHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{Tx}	TxRDY Delay from Center of Data Bit		16	t_{CY}	C_L = 50 pF
t_{Rx}	RxRDY Delay from Center of Data Bit		20	t_{CY}	
t_{IS}	Internal SYNDET Delay from Center of Data Bit		25	t_{CY}	
t_{ES}	Internal SYNDET Set-Up Time Before Falling Edge of RxC		16	t_{CY}	
t_{TxE}	TxEMPTY Delay from Center of Data Bit		16	t_{CY}	C_L = 50 pF
t_{WC}	Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)		16	t_{CY}	
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		16	t_{CY}	

3. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1x Baud Rate, f_{Tx} or $f_{Rx} < 1/(30\ t_{CY})$
   For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} < 1/(4.5\ t_{CY})$

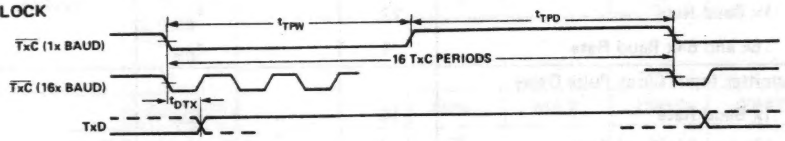
4. Reset Pulse Width = 6 t_{CY} minimum.

READ AND WRITE TIMING

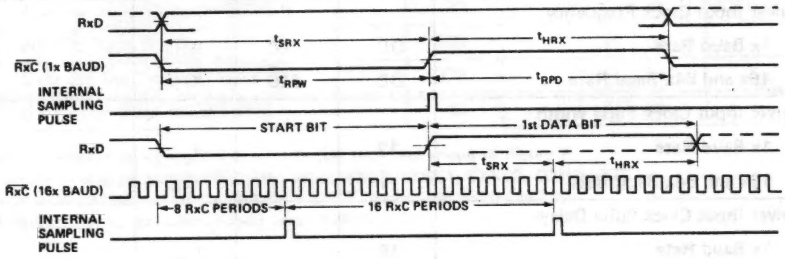


*WRITE AND READ PULSES HAVE NO TIMING LIMITATION WITH RESPECT TO CLK.

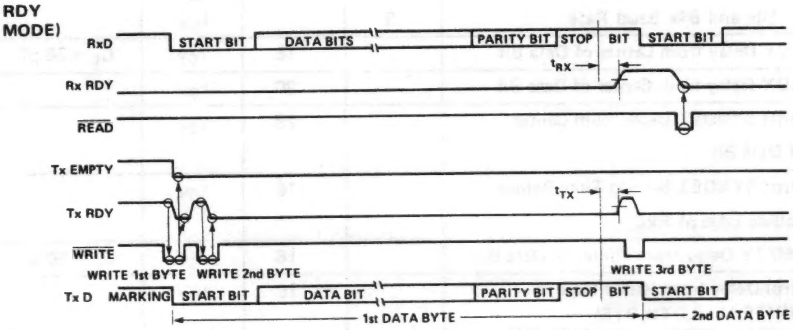
TRANSMITTER CLOCK AND DATA



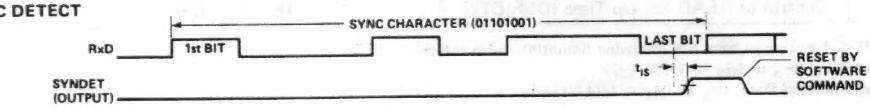
RECEIVER CLOCK AND DATA



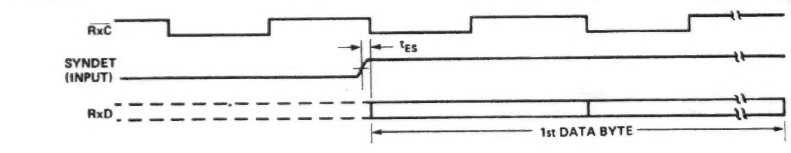
Tx RDY AND Rx RDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT



DTE		DCE	Name
1		1	Prot gnd
2	Tx data →	2 ←	Tx data
3	Rx data ←	3 →	Rx data
4	RTS →	4 ←	Request to send.
5	CTS ←	5 →	clear to send
6	DSR ←	6 →	Data set ready.
7	gnd	7 gnd	Sig ground
8	DCD ←	8 →	Data Carrier detect
–	+ve] do not connect	– +ve (	Aux Supply Volts. don't connect
–	-ve]	– -ve (	
11	Sel ch. →	11 ←	Select work ch 1/2.
–		–	
–		–	
–		–	
–		–	
–		–	
–		–	
18	Anal loop →	18 ←	initiate analogue loop back.
–		–	
20	DTR →	20 ←	Connect to line
			Data Term. Ready.
21		21	
			Dig loop test
			Quad indicator
22	RI ←	22 →	Ring indicator
–		–	
–		–	
–		–	

NB

3802 thinks its a DCE not DTE.